REMARKS

Preliminary Amendment May or May Not Have Been Considered

The Office Action Summary does not indicate to which communication the Office Action is responsive. Therefore, it is not clear to Applicant whether the Preliminary Amendment filed on February 1, 2005 has been considered.

Because the Office Action appears to ignore some limitations in some of the claims, Applicant postulates that the Preliminary Amendment has not been considered. Therefore, Applicant respectfully requests that receipt and entry of the Preliminary Amendment be confirmed in the next communication from the Patent Office.

Oath/Declaration

The Office Action states:

> Applicant has not given a post office address anywhere in the application papers as required by 37 CFR 1.33(a), which was in effect at the time of filing of the oath or declaration. A statement over applicant's signature providing a complete post office address is required.

Applicant respectfully draws to the Examiner's attention the Application Data Sheet that was filed with the application, and with the declaration signed by Applicant. The Application Data Sheet includes the full post office address of Applicant. Further, Applicant's representative verified on June 9, 2005 via the PAIR system that the Application Data Sheet was received by the PTO and was scanned into the system.

37 CFR 1.33(a) states:

> When filing an application, a correspondence address must be set forth in either an application data sheet (§1.76), or elsewhere, in a clearly identifiable manner, in any paper submitted with an application filing.

Therefore, Applicant has fully complied with the requirements of 37 CFR 1.33(a).

Objection to the Drawings

Applicant has amended paragraph [0038] to include a reference to element 313 of Figure 3 as required by the Office Action. The objection to the drawings is therefore

overcome.

These amendments merely bring the specification into conformance with Figure 3. Therefore, no new matter is added.

Objections to the Claims

Claims 21 and 23 are objected to because of the wording "an PMOS". This phrase has been corrected in each of Claims 21 and 23 to read "a "PMOS", as required by the Examiner.

Please note that the amendments to Claims 21 and 23 merely correct a minor grammatical error. Therefore, these amendments are not narrowing and are not made for the purpose of patentability or avoiding the prior art.

Claims 3-4, 7-8, 11-12, and 15-16 are objected to as being dependent from a rejected base claim, but otherwise allowable. Applicant thanks the Examiner for this acknowledgement of allowable subject matter. However, Applicant believes that all rejections are overcome by the remarks below, and that these objections have therefore been overcome.

Summary of Claim Status

Claims 1-23 are pending in the present application after entry of the present amendment. Claims 1-2, 5-6, 9-10, 13-14, and 17-25 are rejected for the reasons discussed below.

Claims 3-4, 7-8, 11-12, and 15-16 are objected to as depending from a rejected base claim, but would be allowable if properly rewritten in independent form.

Applicant requests the favorable reconsideration of the claims and withdrawal of the pending rejections and objections, in view of the present amendment and in light of the following remarks.

Rejections Under 35 USC 102(e)

Claims 1-2, 5-6, 9-10, 13-14, and 17-25 are rejected as being anticipated by Tomishima (U.S. Patent No. 6,807,109, hereinafter Tomishima). The Examiner

therefore argues that Tomishima teaches every element of every claim, either expressly or by implication. (MPEP 706.02, pg. 700-20, provides the following summary of the relevant standard: "For anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present.") Applicant respectfully disagrees.

Claims 19-21

The Office Action states:

> Regarding to claims 19-21, Tomishima discloses a memory cell for suppressing sub-threshold leakage in a transistor, the memory comprising: a plurality of transistors (27, 28, 200a, 200b) configurable to store a value...

Applicant is confused by this characterization of the reference. Tomishima does not appear to disclose or address memory cells. In particular, elements 27, 28, 200a, and 200b are not memory cells and do not comprise any portion of a memory cell. Elements 27, 28, 200a, and 200b are output transistors coupled to an output node OPD (column 12, lines 44-49; column 11, line 51). Therefore, transistors 27, 28, 200a, and 200b clearly cannot store a value. Therefore, clearly Tomishima neither teaches nor suggests that "the value can under-drive the transistor in its off state" as claimed in Claim 19. Further, Tomishima does not appear to address the issue of suppressing sub-threshold leakage.

Further in regard to Claim 19, the Office Action states:

> [Tomishima's] memory comprising: a plurality of transistors (27, 28, 200a, 200b) configurable to store a value, wherein the value can drive the transistor in its off state, wherein if the transistor is an NMOS device having source voltage of VSS and the memory cell drives a gate of the transistor, then the value of (*sic*, is) slightly more negative then (*sic*, than) VSS (Vbb); if the transistor is a PMOS device having a source voltage of VDD and the memory cell drives a gate of the transistor, then the value of (*sic*, is) slightly more positive than VDD (Vpp). *See Figs 8-10, 39-41; Cols. 15-18, 39-41.* (emphasis original)

The Office Action has not proven that Tomishima teaches or suggests "the value can under-drive the transistor in its off state." Further, it is unclear what "value" of Tomishima's is referred to in the rejection quoted above. For example, Tomishima shows "values" VNW and VPW driving the wells of transistors 27 and 28, respectively (Figs 8-10, 39-41), and each of these values can have one of two voltages. However, these wells do not "drive the transistor". As is well known to those of skill in the art, the term "driving a transistor" refers to providing a voltage to the gate of the transistor. On the contrary, Tomishima addresses applying one of two values to the well of a transistor. For example, "Fig. 8 schematically shows a configuration of a portion of second output buffer 10 for applying a well (back gate) bias." Col. 15, lines 44-45.

Therefore, there appears to be no correlation between the transistors identified in the reference by the Office Action and the transistors in Applicant's Claim 19.

Therefore, Claim 19 distinguishes over Tomishima for at least these reasons. Claims 20-23 also distinguish over Tomishima for at least the reasons of Claim 19, from which they depend.

Claims 22-23

The Office Action further states:

> Regarding to claims 22-23, wherein if the transistor is an NMOS device having a gate voltage of VSS and the memory cell drives a source of the transistor, then the value is slightly more positive then (*sic*, than) VSS (VFRP); if the transistor is a PMOS device having a gate voltage of VDD and the memory cell drives a source of the transistor, then the value is slightly less than VDD (VFRN). *See Figs 8-10, 39-41; Cols. 15-18, 39-41.* (emphasis original)

Tomishima does not show a memory cell driving the source of any transistor in the cited figures, or reference such a memory cell in the cited text. Therefore, the Office Action fails to prove that Tomishima shows either Applicant's claimed "wherein if the transistor is an NMOS device having a gate voltage of VSS and the memory cell drives a source of the transistor, then the value is slightly more positive than VSS" (Claim 22) or Applicant's claimed "wherein if the transistor is a PMOS device having a gate voltage of VDD and the memory cell drives a source of the transistor, then the value is

slightly less than VDD" (Claim 23).

Therefore, Claims 22-23 further distinguish over Tomishima for at least these reasons.

Claims 24-25

Claims 24 and 25 are also rejected over Tomishima. Applicant has cancelled Claims 24 and 25. Therefore, this rejection is moot.

Claims 1-2, 5-6, 9-10, 13-14, 17-18

Regarding Claims 1-2, 5-6, 9-10, 13-14, and 17-18, the Office Action simply includes a broad, conclusory statement:

> With regard to method claims 1-2, 5-6, 9-10, 13-14, 17-18, they encompass the same scope of invention as to that of claims 19-25 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

This statement completely ignores many limitations present in the claims. For example, none of Claims 19-25 includes a set of limitations that exactly corresponds to those of Claim 1. Claim 1 includes limitations directed to "storing a value in a memory cell coupled to a gate of the transistor" and "applying a gate to source voltage to the transistor that under-drives the transistor", neither of which are included in Claims 19-25. Claim 19 specifies that the circuit "can under-drive the transistor in its off state." Claims 20-24 include specific limitations regarding NMOS and PMOS devices. Claim 25 specifies that the circuit "creates a negative gate to source voltage when the transistor is in its off state." None of these limitations are included in Claim 1. This is just one of many examples illustrating that it is inappropriate to apply a broad rejection to all of the method claims based on the rejection of structural Claims 19-25.

Applicant respectfully requests that, if the rejection is maintained, the next Office Action include specific recitations of portions of the cited reference that anticipate the limitations of each of Claims 1-2, 5-6, 9-10, 13-14, and 17-18.

Request for Non-Final Action

If an action other than allowance of the pending claims is to be made, Applicant respectfully requests that the next action be a non-final action.

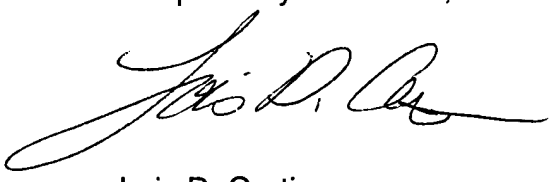
The outstanding Office Action apparently does not take into account the Preliminary Amendment filed February 1, 2005, four months prior to the mailing date of the outstanding Office Action.

Further, MPEP 707.07(d) states that "a plurality of claims should never be grouped together in a common rejection, unless that rejection is equally applicable to all claims in the group." As apparatus and method claims have been grouped together without explanation, Applicant hereby requests a new non-final action if the pending claims are not allowed.

Conclusion

No new matter has been introduced by any of the above amendments. All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested. If any action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicant's agent, Lois D. Cartier, at 720-652-3733.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on June 21, 2005.

Pat Slaback
Name

Signature